Semiconductors

1) Sketch the energy band diagram (E versus x) including Fermi level of an intrinsic semiconductor under uniform electric field in x-direction.

2) Sketch the energy band diagram of a moderately and uniformly doped n-type silicon, clearly showing the location of the phosphorus impurity level, Fermi-level and Intrinsic level at room temperature. On the diagram, mark the Energy differences (E_c - E_v) and ($E_f - E_i$) for a doping level of 1×10^{15} cm^{-3}, assuming intrinsic concentration of 1×10^{10} cm^{-3} at room temperature.

3) What are the factors which affect the ionization coefficient (η) in a doped semiconductor? How do change (increase/decrease) in these factors affect (i.e. increase/decrease) the value of η?

4) A silicon sample is doped with 10^{18} donor atoms per cm^3. The position of the Fermi level for this sample is $E_F = E_i + 0.45$ eV at 300 K. What fraction of the donors is ionized in this semiconductor?

5) The position of the Fermi level for a silicon sample is at $E_F = E_i - 0.35$ eV at 300 K. The sample is uniformly illuminated, thereby generating an additional 10^{18} electron-hole pairs per cm^3 per second. If the minority carrier lifetime in this sample is 1 μs, what are positions of the quasi Fermi levels at 300 K for this illuminated sample?

6) The Fermi level in a semiconductor bar should

   A) be constant as a function of distance, under equilibrium
   B) be constant as a function of distance, under both equilibrium and non-equilibrium conditions.
   C) vary with distance under equilibrium
   D) vary with distance under both equilibrium and non-equilibrium conditions.

7) When the temperature is increased, the position of the Fermi level in an n-type semiconductor

   (A) moves towards the conduction band edge
   (B) moves towards the valence band edge
   (C) moves towards the middle of the band gap
   (D) remains unchanged

8) When the donor impurity concentration in an n-type semiconductor is increased, the position of the Fermi level

   (A) moves towards the conduction band edge
   (B) moves towards the valence band edge
   (C) moves towards the middle of the band gap
   (D) remains unchanged

9) As the temperature is increased from 0 K, the mobility of a moderately doped semiconductor shows

   A) a decrease followed by an increase
   B) an increase followed by decrease
   C) a monotonic increase
   D) a monotonic decrease

10) A silicon sample A is doped with 10^{17} phosphorus atoms/cm^3 and sample B is doped with 10^{17} boron atoms/cm^3. Which of the two samples has a higher resistivity?

11) A phosphorus doped (10^{17} atoms/cm^3) Si sample has resistivity of 0.1Ω-cm. Calculate the doping concentration of boron atoms if it is additionally used to reduce the resistivity of this doped sample by 50%. Assume that due to this additional boron doping electron mobility is not reduced further and in the final sample it is three times of the hole mobility.

12) Estimate the room temperature hole concentration and resistivity in a silicon sample with 10^{15} cm^{-3} phosphorus atoms, taking hole mobility = 400 cm^2 / V-s, electron mobility =1000 cm^2 / V-s and intrinsic concentration = 1 x 10^{10} cm^{-3}.

13) A silicon sample is doped with 10^{16} phosphorus atoms/cm^3. Assuming complete ionisation, find out the resistivity of the sample at 300K considering the electron mobility in silicon to be 1350 cm^2/V-sec and the hole mobility 450cm^2/V-sec.

14) A current of 1 mA flows through a bar of uniformly doped n-type silicon with a cross sectional area of 2 mm x 2 mm and a length of 1 cm when it is connected to a 3 V battery at 300K. Calculate the electron and hole concentrations in the bar.

15) Indicate whether the statement given below is TRUE or FALSE.

A metal contact to any heavily doped semiconductor usually results in an ohmic contact.

16) What is the most common acceptor type impurity in silicon?

P-N Junctions

1) Draw the energy band diagrams of an abrupt p-n junction diode when the diode is (a) in thermal equilibrium, (b) forward biased by V_f and (c) reverse biased by V_r. In each figure, show the position of the Fermi level or quasi Fermi levels along with their energy difference, whichever is applicable. Also show the difference in the energies of the conduction band edges of the p-region and n-region in all the cases (The built-in potential is V_{bi}).

2) Acceptor and donor concentration of an abrupt PN-junction are $N_a=4\times10^{18}$/cm^3 and $N_d=4\times10^{17}$/cm^3. Sketch (in scale) the electric field distribution from $-X_{p0}$ to $+X_{n0}$ considering the metallurgical junction at the origin. X_{p0} and X_{n0} are the penetration depth of the space charge region in P and N regions, respectively. Consider $X_{n0}=0.5\mu$m, and electric field at the metallurgical junction, $E_0 = -3.48$V/μm.

3) A p-n junction under a forward bias of 0.4V has a depletion width of W = 0.1μm. Calculate the peak electric field $\mathcal{E}_{peak}$ in V/cm. Given the built in potential $V_0 = 0.8$V.

4) The figure below shows the electric field profile for a reverse biased p-n junction.
(a) If the doping concentration on the p-side is 10^{17}/cm^3, what is the doping concentration on the n-side?
(b) If the built-in potential of the p-n junction is 0.75 V and the applied reverse bias is 5.25 V, what is

magnitude of the maximum electric field (E_m)?
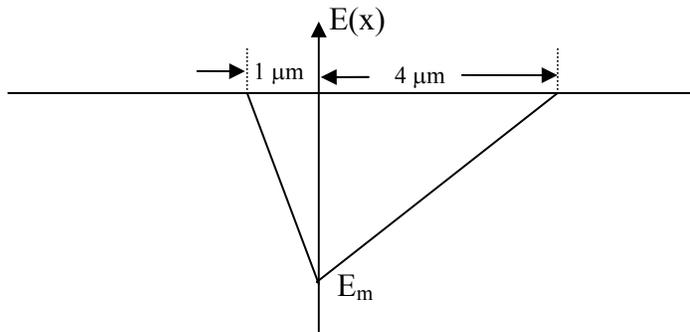
5) If the depletion layer width in a reverse biased abrupt p-n junction is 1 μm when the voltage across the depletion layer is 1 V, what will be the depletion layer width when the reverse bias across the abrupt p-n junction is increased to 4 V?

6) In a p-n junction, the doping concentrations in the p and n regions are given by $N_A = 10^{17}/cm^3$ and $N_D = 10^{16}/cm^3$ respectively. If the depletion layer width on the n-side is 1 μm, what will be the depletion layer width on the p-side?

7) The built-in potential of a p-n junction is 0.8 V. The depletion capacitances of the junction at a forward bias of 0.7 V and a reverse bias of 0.8 V are $C_{0.7f}$ and $C_{0.8r}$ respectively. Find out the ratio $C_{0.7f}/C_{0.8f}$.

8) The depletion layer width (W) for a reverse biased abrupt p^+-n junction is 1 μm and the depletion (or junction) capacitance (C_J) is 10 pF when the voltage across the depletion layer ($V_{bi} + V_r$) is 0.75 V. What are the values of W and C_J when ($V_{bi} + V_r$) is 3 V?

9) A silicon abrupt p^+n junction diode has a built-in potential of 0.8 volts. At a reverse bias of 3.2 V, the depletion capacitance is 100pF. What is the value of the reverse bias at which the capacitance will become 50 pF?

10) The built-in potential of an abrupt p-n junction is 0.75 V. If the depletion layer width (W) and junction capacitance (C_J) are 1 μm and 10 pF when the reverse bias (V_r) is 1.25 V, what are the values of (a) W and (b) C_J when V_r is 31.25 V?

11) Reverse saturation current, non-ideality factor, and room-temperature thermal voltage of a long p^+-n junction diode are 1.12pA, 1, and 0.025V, respectively. If at room-temperature, diffusion capacitance at a forward current of 0.1mA is found to be 10pF, find out hole lifetime (τ_p) within the n-region.

12) If the reverse saturation current, non-ideality factor, and room-temperature thermal voltage of a p-n junction are 1.12 pA, 1, and 0.0259 V, respectively, find out the room-temperature a.c. resistance of the diode at a forward current of 0.1mA.

13) Find out the forward biased p-n junction diode current (in mA) at which its room temperature (T = 300K) a.c resistance is 250 Ω. Assume that the reverse saturation current is of the order of pA. Given non-ideality factor η = 1, Boltzmann's constant k = 1.38×10^{-23} J/K, electron charge q = 1.6×10^{-19}C.

14) Plot diode conductance versus forward diode current assuming reverse saturation current, I_0=0.5nA and thermal voltage V_T=0.0259V.

15) Draw the forward and reverse I-V characteristics of a 7 V zener diode *approximately to scale*, showing whether the voltage axis is in nV, μV, mV or V, and the current axis is in nA, μA, mA or A.

16) In a p-n junction diode, the diffusion length of holes in the n-side is 30 μm. If x = 0 is at the edge of the depletion region on the n-side and x = W_n is at the n-contact, show the nature of hole concentration profile p(x) from x = 0 to x = W_n when the diode is forward biased if (a) W_n = 2 μm and (b) W_n = 400 μm.

17) Two p-n junction diodes D1 and D2 are identical in all respects except that D1 is made of a wider bandgap material than D2. The reverse saturation current will be maximum for

(A) D1 operating at 100°C   (B) D2 operating at 100°C
(C) D1 operating at 30°C   (D) D2 operating at 30°C

18) Two p^+n diodes D3 and D4 having short n-regions are identical in all respects except that the width of the n-region in D3 is double that in D4. If the current in D3 is 1 mA at a forward bias of 0.6 V, what will be the current in D4 at the same bias?

19) In their normal mode of operation, (choose the correct answer)
(A) a LASER is forward biased and a photodiode is reverse biased
(B) a LASER is reverse biased and a photodiode is forward biased
(C) both LASER and photodiode are forward biased
(D) both LASER and photodiode are reverse biased

20) In their normal mode of operation,
(A) a LED is forward biased and a Zener diode is reverse biased
(B) a LED is reverse biased and a Zener diode is forward biased
(C) both LED and Zener diode are forward biased
(D) both LED and Zener diode are reverse biased

Bipolar Junction Transistors

1) Will two diodes connected back-to-back behave as a transistor? Justify your answer.

2) Sketch the minority carrier distribution in the base of a BJT biased in the (a) forward active and (b) saturation regions.

3) Draw the output characteristics of a BJT in (a) common emitter and (b) common base configurations and show the saturation, active and cut-off regions.

4) In normal active mode an n-p-n bipolar transistor is assumed to have emitter injection efficiency γ = 1 and negligible holes entering from collector into base. If the transit time and life time of electrons in the base region are found to be 10 ns and 0.99 μs, respectively, find out on an average

how many electrons will recombine inside the base for every 1000 electrons injected from emitter.

5) Pick the correct statement :

To increase the β of a bipolar transistor
(A) the base width or doping concentration in the base should be increased
(B) the base width or doping concentration in the base should be reduced
(C) the base width should be reduced and doping concentration in the base should be increased
(D) the base width should be increased and doping concentration in the base should be reduced

6) The emitter efficiency and base transport factor in an n-p-n bipolar transistor are 0.99 and 0.98 respectively. What is the β of this transistor?

7) The β of an npn transistor is estimated to be 150 considering only the effect of emitter efficiency (γ) and assuming base transport factor (α_T) =1. On the other hand, considering only the effect of α_T and assuming γ =1, the β of the same transistor is found to be 120. What is the actual β of the transistor if both α_T and γ are taken into account?

8) The β of an npn bipolar junction transistor (BJT) is 50. If the base transport factor (α_T) = 0.99, then what is the emitter efficiency (γ)?

9) The β of an npn BJT is 78. If it is biased in the normal active mode in the common emitter configuration, what is its transconductance (g_m) at room temperature (300K) when base current (I_B) = 10μA?

10) Assume that collector current of an npn bipolar transistor is approximated as

$$i_C = I_C(d.c.) + i_c(a.c.) = I_S \exp\left(\frac{V_{BE} + v_{be}}{V_T}\right)$$

where I_S is the saturation current, V_{BE} is the base-emitter bias voltage, and v_{be} is the small-signal a.c. voltage at the base. In a common emitter configuration, plot the small-signal trans-conductance (g_m) versus operating d.c. current $I_C(d.c.)$.

11) Indicate whether the highlighted portion of the statement given below is TRUE or FALSE.

In a conventional npn BJT, **the breakdown voltage of the emitter-base junction is usually much greater than the breakdown voltage of the collector-base junction**.

MOSFETs

1) Fig. 1 shows the C-V characteristics of a metal-oxide-silicon (MOS) capacitor. Pick the correct statement below:
(A) The substrate is n-type and the measurement is done at low frequency.
(B) The substrate is p-type and the measurement is done at low frequency.
(C) The substrate is n-type and the measurement is done at high frequency.
(D) The substrate is p-type and the measurement is done at high frequency

2) Fig. 1 shows the C-V characteristics of a metal-oxide-semiconductor (MOS) capacitor with an area of $1.5mm^2$. What is the maximum depletion layer width (W_{max}) in μm?
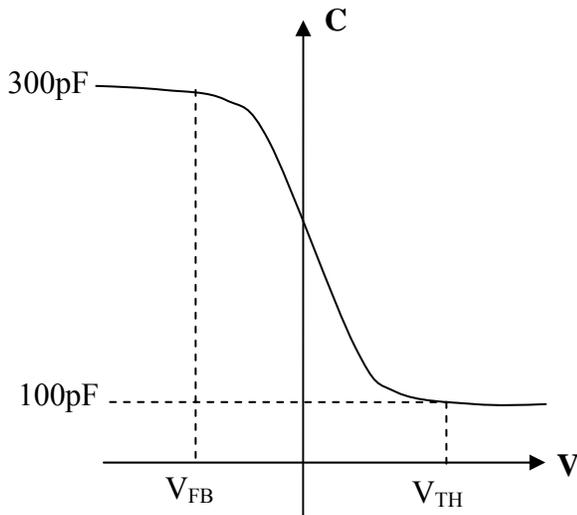

Fig. 1

3) In Fig.2, if the area of the capacitor is 1 mm^2,
   (a) what is the gate oxide thickness (t_{ox})?
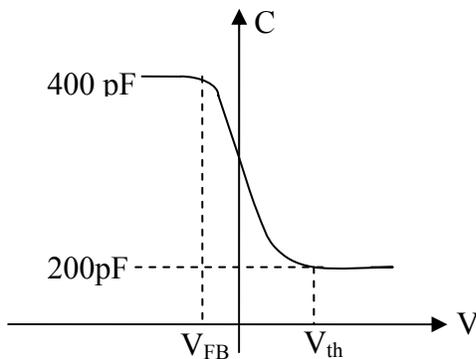   (b) what is the maximum depletion layer width (W_{max})?

Fig.2

4) If the area of a MOS capacitor is 1 mm^2 and the gate oxide thickness (t_{ox}) is 100nm,
   (a) what is C_{max}?
   (b) if $C_{min} = \frac{1}{2}C_{max}$, what is the maximum depletion layer width (W_{max})?

5) A MOS capacitor has an area of 2×10^{-3} cm^2. The substrate doping concentration is $10^{16}/cm^3$. If the maximum and minimum capacitances of the MOS capacitor are 350 pF and 200pF respectively, what is the maximum depletion width?

6) In a metal/SiO_2/p-Si MOS capacitor, the SiO_2 layer thickness is t_{ox} and the doping concentration of the p-type substrate is N_A. The threshold voltage of the MOS capacitor will definitely increase if
   (A) t_{ox} is decreased and N_A is increased   (B) t_{ox} is increased and N_A is decreased
   (C) both t_{ox} and N_A are decreased   (D) both t_{ox} and N_A are increased.

7) Draw the cross-sectional view of an n-channel MOSFET and label the different regions. Explain the operation of the MOSFET with change in drain and gate voltages.

8) Draw the drain current versus drain voltage characteristics of an n-type MOSFET for three different gate voltages. Clearly show the saturation and ohmic regions, and the relative spacing between the saturation segments of the curves assuming equal increments in gate voltage.

9) The threshold voltage (V_{TH}) of an n-channel MOSFET is 1V. If the drain current (I_D) is 10μA when drain-to-source voltage (V_{DS}) is 3V and gate-to-source voltage (V_{GS}) is 2V, find out the value of I_D in μA when $V_{DS} = V_{GS} = 4V$.

10) An n-channel MOSFET with threshold voltage (V_{th}) of 1 V has its gate shorted to drain as shown in the figure. If the drain current (I_D) = 2 mA when V_{DS} = 2 V, what is I_D when V_{DS} = 4 V?
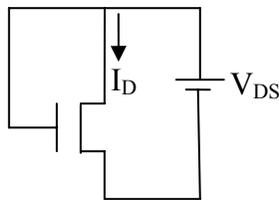

Fig. 3

11) A MOSFET with with threshold voltage (V_{Th}) of 1V has its gate and drain tied together and is used as a voltage variable resistor. A d.c resistance ($R = I_D/V_{DS}$) of 1KΩ is seen between source and drain when $V_{DS} = V_{GS}$ = 10V. What is the value of R when $V_{DS} = V_{GS}$ = 5V.

12) In an n-channel MOSFET having a threshold voltage (V_{th}) of 1 V, the drain current (I_D) is 2 mA when $V_{GS} = V_{DS}$ = 2V, where V_{GS} and V_{DS} are the gate-to-source voltage and drain-to-source voltage respectively. What is I_D when V_{GS} = 4 V and V_{DS} = 2V?

13) Indicate whether the highlighted portions of the statements given below are TRUE or FALSE.
   (a) In an n-channel MOSFET, **the threshold voltage increases with increase in gate oxide thickness**. (Assume oxide charges to be negligible).
   (b) In an n-channel MOSFET, **the minimum subthreshold slope which may be achieved is about 30mV/decade**

[Assume the following data wherever necessary : μ_n = 1350 cm²/V-sec, μ_p = 450 cm²/V-sec, N_C = 2.8 × 10¹⁹ /cm³, N_V = 1 × 10¹⁹ /cm³, E_G = 1.1 eV, n_i = 1.5 × 10¹⁰ /cm³ and kT = 26 meV at 300 K, ε_r = 11.9 for Silicon, ε_r = 3.9 for Silicon Dioxide and ε_0 = 8.85 × 10⁻¹⁴ F/cm.]